

High-End

Video Wall Controller



AIO FPGA VIDEOWALL CONTROLLER



Hardware Based Design

High performance video processing equipment with hardware architecture design.

- ★ No more computer high-end specification.
- ★ No more high-end Graphic Processing Unit (GPU Card).
- ★ No more licenses.
- ★ No more blue-screen OS crash.
- ★ No more viruses and black screen.
- ★ No more ransomwares, lost data.
- ★ Support up to 92 input x 72 output or 88 input x 60 output

FPGA Dedicated Chipset

Dedicated Field Programmable Gate Array (FPGA - Tritium™ 2ndgen - 2280 Gbps) chipset is a combination of processing unit that dedicated in video signal.

This eliminated the limitation of a CPU or a GPU from conventional Software or PC controller. The unit supports 24/7 working time with over 60,000 hours MTBF.

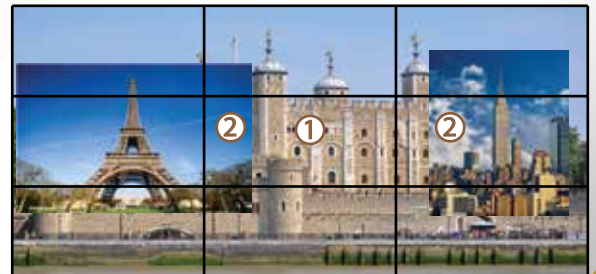
Without the use of PCI - Express card, the unit can work flawlessly when adding or editing the total layout of the videowall set up. As each of the FPGA chip is working independently, user can replace or add new input / output card without turning off the whole chassis.



Module design with Hot Swap

Multiple form of connections for client to custom fit their system. Client can now combine HDMI - DVI - VGA - HDBaseT - IP Streaming in one total solution, maximizing system integration for IT rack (19").

Reduce the total cost of investment in both pre & post phase of expansion. Chassis also support control multiple videowalls, further simplify the complexity of connections and management.



Features

- **High-end 2 up to *4 Layers MPiP™ - Cross Screen**
Support 2 Layers MPiP™, up to *4 Layers-Matrix Picture in Picture (MPiP™) in each screen
- **Easy control with Drag & Drop**
Customize complex layout with simple Click - Drag - Drop
- **High-end Video Wall Control**
Support Overlap, Roaming, Stretching, Zoom in / out.
- **Front Panel Touch Screen**
Control scene mode, save / recall profile (up to 32), IP setting with just a touch
- **IP Camera Direct Stream (iDirect Stream™)**
IP input Card can support streaming video feed direct from IP CCTV Cameras.
- **Background Image - Scrolling Text - Scheduling**
Support Static Background Image and Scrolling Text for Bank and Stock house Video Wall
Support scene mode Scheduling - Cycle for advertising - digital signage Video Wall

VIDEO WALL CONTROLLER - AIO Series

04 x 08 Cross Screens Video Wall

FEATURES

- Pure Hardware Structure - FPGA
- All In One - Hot swap - Hybrid I/O
- Seamless Switching - Auto EDID - 5ms
- Bezel Compensation with Scaler
- Multiple users / rights management
- Character Superimposition, Scrolling Text (opt)
- Multiple video wall management - up to 4
- Signal preview - WEB GUI control (opt)
- Control Room Mode with over IP KVM system extension
- High-end 2 Layer up to *4 Layers MPiP™



SPECIFICATION

Start up time	10s
Switching time	5ms
Chassis size (mm)	1U
Max Data Rate	15.2 Gbps (3.8Gbps per Lane)
Input Interface Port	04
Output Interface Port	08
Interface Support (Input / Output)	HDMI
Total number of Input / Output channel	256 channel 4K / 512 channel 1080p with Smart Management Grouping

Control	Over IP / RS-232 / WEB GUI (opt)
HDMI version	1.3 - Support 3D , Deep Color
HDCP version	1.4 / 2.0 / 2.2
Distant support	18-300m with AOC cables / Extenders
Resolution Input / Output (8 Bit RGBA color)	1280 x 720 @ 120Hz 1920 x 1080 @ 60Hz 1920 x 1200 @ 60Hz

Processing chipset	FPGA - Tritium™ 2 nd gen
Screen layer	2 Layers - *Up to 4 Layers MPiP™
Hot-swap EDID	Support Auto EDID
Power Supply	Main - Support Redundant (OPT)
Interface link	Analog - Digital - IP Stream

Output restriction	Support all type of display (Screens / Projectors / DLP / LED)
Mobile Control	Support iOS & Android
One click ON/OFF	Support

Pixel Clock	225 Mhz
HDMI impedance	100 Ω - ESD Protection
Power Rating	100-240 VAC; 50/60Hz
Power Consumption	100 - 450 W
Fan Airflow	55 - 65 cfm (12VDC)
Operating Temperature	-20 ~ 70°C
Storage Temperature	10 ~ 90°C
Storage / Operating Humidity	5~95% RH (without condensation)

*4 Layers MPiP™ configuration will allocate double output video bandwidth on each port, the total number of output operational ports will be reduced in half.

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